IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Application of:	)
Applicant(s): Hiroshi Murakami	)
Serial No.: 09/314,750	)
Conf. No.: 5601	)
Filed: May 19, 1999	)
For: DISPLAY DEVICE HAVING REDUCEDNUMBER OF SIGNAL LINES	)
Art Unit: 2674	)
Examiner: Lesperance, J.	)

I hereby certify that this paper is being deposited with the United States Postal Service as FIRST-CLASS mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this date.

April 11, 2005
Date

Attorney for Applicant(s)
Registration No. 47,954

RESPONSE TO NOTIFICATION OF NON-COMPLIANT APPEAL BRIEF

Mail Stop APPEAL BRIEF-PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Notification of Non-Compliant Appeal Brief, mailed March 9, 2005, please consider the following remarks:

REMARKS

Appellants respectfully traverse the Notification of Non-Compliant Appeal Brief as being inapplicable to the Appeal Brief filed in this case on December 10, 2004. Almost all of the Rule 41.37 provisions marked by the Examiner in the Notification are erroneous. Appellants submit that the Examiner may have meant to file the Notification in relation to a different case.

For example, the Examiner asserts (Provision No. 8) that the Brief does not contain copies of evidence submitted under 37 C.F.R. 1.130, 1.131, or 1.132, or of any other evidence entered by the Examiner and relied upon by Appellant in the Appeal. No such evidence, however, has been submitted under any of the cited C.F.R. sections, or otherwise by the Examiner and relied upon by Appellants in this Appeal. The Examiner has provided no explanation for what "evidence" he considers missing from the Brief. Appellants submit that the Notification is improper for at least these reasons.

Similarly, the Examiner further asserts (Provision No. 9) that the Brief does not contain copies of decisions rendered by a court or the Board in the proceeding identified in the Related Appeals and Interferences section of the Brief. No such proceedings, however, were identified in the Related Appeals and Interferences section of the Brief. In fact, this section of the Brief unequivocally states that "there are no related appeals or interferences" with respect to this Appeal. The Examiner has provided no other explanation for the assertion, and Appellants therefore submit that the Notification is improper for at least these reasons as well.

With respect to Provision No. 4, Appellants submit that the Examiner's assertions thereto also render the Notification improper. There is only one independent claim on appeal in the present case, and specific references to the Specification and drawings (Provision 4(a)) were omitted as being unduly cumbersome. The subject matter of independent claim 2 of the present invention is described throughout the majority of the entire Specification, and appears in almost all of the drawings as well. Nevertheless, in order to expedite this Appeal and assist in the Examiner's understanding of the present invention, Appellants have revised the Summary of the Invention section of the Appeal Brief, submitted herewith in the Substitute Brief on Appeal, to reference at least the first such occurrences in the Specification of the subject matter of independent claim 2, and which of the drawings apply. The substance of the Substitute Brief on Appeal is otherwise identical to the original Brief in every respect.

The substance of Provision No. 4(b), on the other hand, is wholly inapplicable to the present case, because there is no means plus function or step plus function language in independent claim 2. Again, the Examiner has provided no explanation justifying his assertion of any of the marked provisions of the Notification, and therefore Appellants submit that the Notification is again improper, and should be vacated.

Respectfully submitted,
GREER, BURNS & CRAIN, LTD.

Customer No. 24978

April 11, 2005

By
Josh C. Snider, Reg. No. 47,954

300 South Wacker Drive
Suite 2500
Chicago, Illinois 60606
Telephone: (312) 360-0080
Facsimile: (312) 360-9315
P:\DOCS\0941\63081\711685.DOC

0941 6981

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Murakami, H.
Serial No.:	09/314,750
Conf. No.:	5601
Filed:	May 19, 1999
For:	DISPLAY DEVICE HAVING REDUCED NUMBER OF SIGNAL LINES
Art Unit:	2674
Examiner:	Lesperance, J.

I hereby certify that this paper is being deposited with the United States Postal Service as FIRST-CLASS mail in an envelope addressed to: Mail Stop APPEAL BRIEF-PATENTS, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this date.

April 11, 2005 JOSH WILKER
Date *Registration No. 47,954*

F-CLASS.WCM
Appr. February 20, 1998

Attorney for Applicant

APPELLANT'S SUBSTITUTE BRIEF ON APPEAL UNDER 37 C.F.R. 1.192

Josh C. Snider
GREER, BURNS & CRAIN, LTD.
300 South Wacker Drive
Suite 2500
Chicago, Illinois 60606
(312) 360-0080

Date: April 11, 2005

TABLE OF CONTENTS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Murakami, H.	)
Serial No.:	09/314,750	)
Conf. No.:	5601	)
Filed:	May 19, 1999	)
For:	DISPLAY DEVICE HAVING REDUCED NUMBER OF SIGNAL LINES	)
Art Unit:	2674	)
Examiner:	Lesperance, J.	)

I hereby certify that this paper is being deposited with the United States Postal Service as FIRST-CLASS mail in an envelope addressed to: Mail Stop APPEAL BRIEF-PATENTS, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this date.

April 11, 2005 *Registration No. 47,954*
Date

F-CLASS.WCM
Appr. February 20, 1998

Attorney for Applicant

APPELLANT'S SUBSTITUTE BRIEF ON APPEAL UNDER 37 C.F.R. 1.192

Mail Stop APPEAL BRIEF-PATENTS
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Appeal Brief is in support of Applicants' Notice of Appeal dated October 13, 2004, from the final rejection dated July 13, 2004.

APPEAL BRIEF

REAL PARTY IN INTEREST

The real party in interest in this case is Fujitsu Display Technologies Corporation, 1-1, Kamikodanaka 4-Chome, Nakahara-ku, Kawasaki-shi, Kanagawa, 211, Japan. An assignment of the Application to the real party of interest has been recorded on Reel 009973, Frame 0829.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences which will directly affect, be directly affected by, or have a bearing on, the Board's decision in this pending appeal.

STATUS OF CLAIMS

This application was originally filed with eleven (11) numbered claims. During prosecution, claim 1 was canceled, and claims 2 and 8 were amended. Claims 2-11 are pending, and stand rejected. The rejection of these claims is appealed. Claim 2 is the only independent claim. Claims 3-4, 6, 8, and 11 depend directly from independent claim 2, and claims 5, 7, and 9-10 depend indirectly from claim 2.

STATUS OF AMENDMENTS

Response G, filed July 13, 2004, has been entered.

Response F, filed December 2, 2003, has been entered.

Amendment E, filed February 6, 2003, has been entered.

Response D, filed June 19, 2002, has been entered.

Amendment C, filed March 4, 2002, has been entered.

Response B, filed August 15, 2001, has been entered.

Response A, filed February 27, 2001, has been entered.

SUMMARY OF THE INVENTION

The present invention relates to an improved liquid crystal display ("LCD") device 100. (Page 5, lines 15-19, et seq.; Figs. 2-4, 6, 8-10). The device 100 distinguishes between memories (MEM90, page 14, lines 3-12, Fig. 8, for example) that store image data and those (MEM1 through $MEM2^m$) that store information regarding control of a display unit of the device, and utilizes one or more operation circuits ($CIR1-CIR2^m$) that control the display unit to display an image based on the display control information stored in the latter memories. (Page 7, lines 18-20, et seq.; Figs. 3-6, 8-14). The present LCD device further connects such display information control memories to the exterior of the device through both the data bus and the address bus, which buses then supply information to the memories, as well as address signals for selecting from the memories, from the exterior. (Figs. 2-6, 8-

10). By such a unique configuration, images of greater complexity may be displayed within a smaller area of the device, but without increasing the number of signal lines typically employed.

According to conventional devices, the number of signal lines required to connect a control device to the LCD device must be equal to at least the total number of bits of all operation circuits employed by the LCD device. Therefore, as the complexity of an image to be displayed is increased, the number of operation circuits/operation circuit bits must also be increased accordingly, thereby resulting in additional signal lines being required to transfer information between the control device and the LCD device. Cost, and complexity of manufacture, of such devices will also undesirably increase.

In contrast, according to the present invention, specific memories are allocated to store information for controlling the display of image data, which is different from the image data itself. The data bus and the address bus of the device are then utilized to connect these memories to the exterior of the device. Information is supplied to these memories from the exterior through the data bus, and address signals are similarly supplied for selecting from these memories. By utilization of these device elements in this way, the number of signal lines needed to display images of greater complexity does not have to increase.

ISSUES PRESENTED

I. Whether claim 2 of the present invention was properly rejected under 35 U.S.C. 102(e) as being unpatentable over Ikeda et al., when the reference does not disclose (or suggest) all of the recited features of the present invention.

II. Whether the Examiner's reliance on inherency was justified, when the Examiner has neither cited to any extrinsic evidence nor any specific teachings from the single prior art reference to support the assertion of inherency.

GROUPING OF CLAIMS

Dependent claims 3-11 stand with independent claim 2. Claims 3-10 also each stand independently from claim 2, if rewritten in independent form.

ARGUMENT

I. THE REJECTION OF CLAIMS 2-11 UNDER 35 U.S.C. 102(e) AS BEING UNPATENTABLE OVER IKEDA IS IMPROPER BECAUSE A *PRIMA FACIE* CASE OF ANTICIPATION HAS NOT BEEN ESTABLISHED AGAINST THE PRESENT INVENTION.

The Section 102 rejection of independent claim 2 based on Ikeda et al. (U.S. 5,502,889) is improper. A *prima facie* case of anticipation has not been established against the present invention based on this single reference. Ikeda does not teach (or suggest) all of the recited features and limitations of the present invention, and portions of the reference asserted by the Examiner to be analogous to particular features of the present invention do not support such assertions.

A. Ikeda Does Not Teach (or Suggest) All of the Claim Limitations of the Present Invention.

Independent claim 2 of the present invention specifically identifies the recited memories of the present invention as those which store information for controlling the display of the image data. Claim 2 further specifically differentiates this information for controlling the display of image data from the image data information itself. It is important to note that Ikeda never makes such a distinction between display control information and image data information. In fact, Ikeda identifies only two distinct memories in its device -- a main memory 1602, and a memory cell 120. Neither of these memories, however, is taught by Ikeda to store information for controlling the display of image data.

Ikeda specifically teaches, at col. 14, lines 59-61, that image display data is transferred through a data bus 1605 from or to the main memory 1602. Ikeda further teaches, at col. 9, lines 45-47, that the memory cell 120 also contains image display data. Ikeda does not otherwise teach that either one of these two memories may also contain *information for controlling* the image display data, which is different from the display data information itself.

Ikeda's CPU 1601 thus remains the only portion of the reference asserted by the Examiner to be analogous to the particular memories of the present invention. It is significant to note, however, that the Examiner does not actually assert that the CPU 1601 is described to include display control memories comparable to those recited in the present invention. Instead, the Examiner only asserts, on page 2 of Paper No. 22, that the CPU 1601 "*may* include a lot of memories which is (sic) different from the main memory" 1602. (Emphasis added). In other words, the Examiner has rejected claim 2 of the present invention only on the mere *possibility* that Ikeda may have features similar to the present invention, but not on any specific teaching from the reference itself. A *prima facie* case of anticipation has therefore not been established.

A finding of anticipation requires the disclosure in a single prior art reference each and every element of the claim under consideration. See W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed Cir. 1983). In the present case, however, this basic requirement has not been satisfied. There is no teaching (or suggestion) within the Ikeda reference itself that particularly describes memories that store information for controlling the display image data comparable to those memories recited in claim 2 of the

present invention. The only factual support for such an assertion on the record therefore, is the Examiner's own personal assertion that such memories "may" be included in Ikeda's CPU. Because Ikeda itself does not actually support such an assertion, the final rejection of independent claim 2 under Section 102 should be reversed for at least these reasons.

This Board should also reverse the final rejection of claim 2 because Ikeda similarly fails to disclose several other recited features of the present invention. In addition to the memories discussed above, claim 2 further recites an operation circuit unit which controls a display unit to display image data based on the display control information stored in the memories, a data bus which connects the memories to an exterior of the device and supplies information to the memories from this exterior, and an address bus which also connects the memories to the exterior of the device, and also supplies address signals for selecting one of the memories. Ikeda does not teach (or suggest) elements analogous to these additionally recited features from claim 2.

It is significant to note that all three of these claim 2 elements – the operation circuit unit, the data bus, and the address bus – are configured, or function, with specific regard to the display control information memories discussed above. The operation circuit unit controls the display unit based on the display control information stored in these memories, and both the data bus and the address bus connect such display control memories to the exterior of the device. Therefore, even if, as asserted by the examiner, the limitations related to the memories themselves of claim 2 could somehow be met by Ikeda's CPU 1601,

there would still have to be some additional teaching within the Ikeda reference for these additional recited features of claim 2. No such teachings, however, exist in the reference.

As discussed above, Ikeda does not actually teach that display control information memories are contained within the CPU 1601. The Examiner only asserts that such memories "may" exist there. There is no teaching in the reference therefore, for an additional operation circuit unit that controls the display unit *based on the display control information* from such memories. Furthermore, there could also be no teaching in Ikeda that such theoretically possible memories are actually connected to the exterior of the device through either a data bus or an address bus.

Even if the Examiner were correct that the CPU 1601 of Ikeda *could* contain such memories as recited by claim 2 of the present invention, Ikeda does not show any address bus or data bus connecting the exterior of the device to such memories in the CPU. Ikeda specifically teaches, at col. 14, line 59, that the CPU 1601 inputs and outputs *image display data*, which is recited in claim 2 of the present invention to be distinct from the information for controlling the display of such data. Ikeda further teaches that the information input to/output from the CPU 1601 *through the data bus 1605* is image display data, and not information for controlling such display data. (See col. 14, lines 59-65). Accordingly, Ikeda fails to teach (or suggest) at least these additional features of claim 2 of the present invention, and therefore this Board should reverse the final rejection of claim 2 for at least these additional reasons.

Furthermore, whether or not Ikeda's CPU 1601 could contain memories for storing display control information, and whether or not such display control information could possibly be transferred through the data bus 1605 that connects the CPU, Ikeda still does not actually teach (or suggest) any such features to its device. Such a clear teaching is a basic requirement for a rejection under Section 102. Ikeda merely discloses the conventional method where image display information is transferred through the data bus (and the address for such image display information similarly transferred through the address bus 1604). There is therefore no description within the single reference that would enable one skilled in the art to produce the distinct memories of the present invention, which store information for controlling the display image data, and which memories connect to the exterior of the device through an address bus and a data bus, and where the information stored in such memories is utilized by the operation circuit unit of the present invention for controlling the display of data on the display unit.

Even giving claim 2 its broadest reasonable interpretation, when this claim is read in light of the Specification to the present Application, the memories of the present invention that store display control information, and all other features of the invention that relate to such memories or their information, do not read upon any of the conventional memories that are actually taught by Ikeda. The memories of the present invention, and the display control information which is stored within them, are sufficiently described to be distinct from anything taught by Ikeda. Accordingly, for these still further reasons, this Board should reverse the Examiner's final rejection of claim 2 of the present invention.

Irrespective of all of the deficiencies in the Section 102 rejection of independent claim 2, this Board should additionally reverse the final rejection of dependent claims 3-10 of the present invention for reasons apart from those discussed above with respect to claim 2. Claims 3-10 all recite additional features of the present invention that are also not taught (or suggested) by the single prior art reference, Ikeda.

Claims 3-5 of the present invention, for example, all feature an additional gate driver and data driver, and respectively recite a shift register, a decoder, and an address counter. All of these three claims clearly recite that all of these common and respective features operate based on the display control information stored in the memories, discussed above. Although Ikeda does generally describe gate drivers, data drivers, shift registers, decoders, and address counters, nowhere does Ikeda specifically teach (or even suggest) that any of these various elements operate based on stored display control information, such information being recited by the present invention as being clearly different from the image display data itself. Accordingly, for at least these reasons, a *prima facie* case of anticipation has not been established against claims 3-5, and this Board should therefore independently reverse the final rejection of these claims as well.

This Board should similarly reverse the rejection of claims 6-7, because a *prima facie* of anticipation has not been established against these claims either. Claim 6 features that the display control information memories store pattern data, and claim 7 features that the operation circuit unit further includes a data-synthesis circuit which combines such pattern data stored in the memories with the display data to generate synthesized pattern data.

Ikeda does not teach (or suggest) any comparable features. The lack of distinction between the display control information and image display information is particularly noteworthy with respect to claim 7, which features a circuit for synthesizing these two types of data. Nowhere does Ikeda describe any such circuit for synthesizing display control information with image display data. Again, Ikeda does not even mention the display control information.

The anticipation rejection of claims 8-10 is similarly deficient. Claim 8 features a display-information acquisition circuit which acquires information about the display unit, and addition display-information memories which store such information about the display unit. Ikeda does not teach (or suggest) any circuit which acquires information about the display unit itself, or a third memory to store such information.

As discussed above, the only memories specifically described by Ikeda are those related to image display data itself. Claim 9 further recites how the acquisition circuit of claim 8 checks the display unit with regard to a defect of the display unit. Ikeda, on the other hand, remains silent regarding the acquisition of any information relating to defects in the display unit. Claim 10 alternatively features how the acquisition circuit of claim 8 acquires information with regard to coordinates of a position at which input is entered on the display unit. Ikeda similarly is silent regarding how any circuit could acquire any input position coordinates from the display unit. There is simply no analogous description in the Ikeda reference for any of these features from claims 8-10, and this Board should therefore reverse the final rejection of claims 8-10 as well.

B. The Cited Portions from the Single Prior Art Reference Do Not Support the Examiner's Analogies to Respective Features of the Present Invention.

Not only does Ikeda fail to anticipate all of the features of the present invention discussed above, many of the elements cited by the Examiner as analogous to the features of the present claims fail to actually support the Examiner's assertions in this regard. This lack of support is particularly significant in light of the fact that the Examiner has failed to rebut most of the meritorious arguments made by Applicant during prosecution traversing the citations to these portions of Ikeda.

With regard to claim 2 specifically, the Examiner asserts that, as shown in Fig. 16 of Ikeda, the data bus 1605 meets all of the limitations of the data bus of the present invention. This assertion, however, is erroneous. Contrary to the Examiner's assertion, Ikeda does not show the data bus 1605 connected to the exterior of the device, such as the liquid crystal panel 32, or even that the data bus 1605 connects to memories that store information for controlling the display of image data in the CPU 1601. First, as discussed above, Ikeda does not expressly teach (or suggest) that the CPU 1601 even contains such memories, as asserted by the Examiner. The Examiner has only asserted that the CPU "may" contain such memories. Second, even if the CPU did contain such memories, Ikeda does not *show or describe* the data bus 1605 actually connecting such memories to the exterior of the display. The *prima facie* case of anticipation is therefore deficient with respect to at least these limitations of claim 2.

The *prima facie* case of anticipation is similarly deficient with respect to the recited address bus of claim 2. The Examiner asserts that Ikeda's address bus 1604, "which is exterior to said display device," is analogous to the address bus of claim 2, which connects the particular memories of the present invention to the exterior of the display device, and also supplies address signals for selecting one of these memories containing display control information. These assertions, however, are erroneous.

First, the Examiner appears to have not considered the actual claim language relating to the address of the present invention. Claim 2 does not merely recite that the address bus "*is exterior to* the display device," as the Examiner specifically notes on lines 7-8 of page 3 of Paper No. 22, but instead that the address bus of the present invention connects the particular memories of the present invention, namely, those which store display control information, *to the exterior* of the display device. Something which connects *to* the device's exterior is different than something which *is* exterior to the device. Applicant submits that the Examiner's assertions in this regard represent a fundamental misreading of the claim language of claim 2, and that the *prima facie* case of anticipation is further deficient for at least these reasons.

Second, the *prima facie* case of anticipation is also deficient with respect to the address bus of the present invention, because Fig. 16 of Ikeda does not show (nor does its accompanying text describe) the address bus 1604 connecting the CPU 1601 to the exterior of the liquid crystal panel 132, let alone any memories for storing information regarding display control that may or may not exist within the CPU 1601. In fact, Ikeda does not teach

that control information is transferred through either the address bus 1604 or the data bus 1605, and even teaches away from such an interpretation.

Ikeda expressly teaches that *image display data* is inputted to or outputted from the CPU 1601 through the data bus 1605 from or to the main memory 1602. (See col. 14, lines 59-61). Ikeda further teaches that the *address information* for the same image display data is transferred through the address bus 1604 from the CPU 1601 to the main memory 1602. (See col. 14, lines 13-14). Ikeda does teach a transfer of a control signal though, but only through the control signal bus 1611, which the Examiner even acknowledges is not part of the address bus 1604 or the data bus 1605. (See col. 14, lines 56-58). In other words, Ikeda only teaches a conventional device, where image display data is transferred through a data bus, its corresponding address information through the address bus, and control information through a control signal bus. Ikeda provides no other teaching or suggestion to enable one skilled in the art to deviate from such a conventional device, to supply control information through one or both of the data bus or address bus, as alleged by the Examiner.

Nevertheless, the Examiner asserts that the information transferred to and from the CPU 1601 "must be" different from image display data, because of Ikeda's teaching, at col. 14, lines 30-33, that the driver memory map when seen from the liquid crystal drivers 105-1 and 105-2 is different from the screen memory map when seen from the CPU 1601. Applicant submits though, that this assertion by the Examiner represents a fundamental misunderstanding of the Ikeda reference. Applicant does not dispute that the driver memory map seen from the liquid crystal drivers 105 is different from the screen memory map seen

from the CPU 1601. Applicant does dispute though, that these two memory maps contain different types of memory information. Ikeda clearly shows that both the screen memory map and the driver memory map contain *image display data information*, and not information for controlling the display of such image display data.

Ikeda illustrates a layout for the screen memory map in Fig. 17A, and the driver memory map in Fig. 17B. A simple comparison of Fig. 17A with Fig. 17B clearly demonstrates that both memory maps contain exactly the same type of information, with just a different *organization* of this one type of image data information between the two different memory maps of the information. Ikeda further confirms this analysis, at col. 14, lines 13-18, by describing that the same image display data address, which is transferred from the CPU 1601 to a liquid crystal controller 1607 is then also converted into an address corresponding to the memory map of the liquid crystal driver 105 after first being input into an address converter 1608. The only difference between the two memory maps is the address conversion process, and not the type of information stored within the two memory maps. Accordingly, Ikeda fails to support the Examiner's assertion that one of the two memory maps must contain information for controlling the display of image data which is different from the image data information itself. The *prima facie* case of anticipation is therefore even further deficient for at least these reasons as well.

Many of the Examiner's *prima facie* assertions of analogous elements in the Ikeda reference are also unsupported with respect to dependent claims 3-10 of the present invention. Applicant has traversed and meritoriously argued against the rejection of each of

these claims individually, and it is noteworthy that the Examiner has not attempted to rebut any of these arguments.

With respect to claim 3 of the present invention specifically, Applicant acknowledges that Ikeda does describe a shift register 205-1, as shown in Fig. 2. However, this shift register 205-1, as cited by the Examiner, is shown by Ikeda to be part of a prior art device, and not part of Ikeda's own structure. The Examiner has not cited to anywhere within the rest of the Ikeda reference for how such a conventional shift register may be employed in Ikeda's own device, and particularly with respect to information stored in memories of even Ikeda's device. More particularly, the Examiner has not pointed to anywhere within the reference to show how such a conventional shift register can operate based on information for controlling the display of image data that is stored in memories for such information, as in claim 3 of the present invention. Without such clear teachings from the prior art reference, a *prima facie* case of anticipation cannot be established against the particular features of claim 3.

The Federal Circuit has clearly established that the picking and choosing of individual claim features in isolation from a single reference is not sufficient to establish a case of anticipation. See W.L. Gore & Associates. "Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." Id. (Emphasis added). In the present case, the Examiner has not satisfied this standard. Even though Ikeda does disclose a shift register, Ikeda does not show such a shift register arranged as in claim 3 of the present invention, where such a shift

register operates based on the display control information stored in the memories. As mentioned above, the Examiner has never rebutted these arguments. Applicant therefore respectfully requests that this Board reverse the Examiner's final rejection of claim 3.

A similar deficiency in the *prima facie* case of anticipation exists with respect to claim 4. Ikeda does generally describe a decoder 118-2 in Fig. 18A, but not arranged as in claim 4 of the present invention. Nowhere does Ikeda enable one skilled in the art to implement a decoder which operates based on display control information stored as in the memories of the present invention. The Examiner has never rebutted these arguments either, and Applicant respectfully requests this Board reverse the final rejection of claim 4 as well.

The anticipation rejection of claim 5 also presents the same deficiency. Ikeda describes an address counter 155 in Fig. 29A, but not an address counter as arranged in claim 5 of the present invention. In fact, Ikeda even specifically teaches away from such an interpretation. Fig. 29A clearly shows that the address counter 155 is part of the driver 150-1, which driver is clearly described by Ikeda to take a memory map only of *the internal memory cell 120*, which is only described to contain image display data. (See col. 9, lines 46-48). The address counter in Ikeda cited by the Examiner therefore, is specifically described by Ikeda to be different from the address counter of claim 5 of the present invention, which is recited to be arranged to operate based on the display control information stored in the particular memories of the present invention. The Examiner has not rebutted any of these arguments as well, and Applicant further requests that the Board also reverse the final rejection of claim 5.

With respect to claims 6 and 7 of the present invention, the anticipation rejection is deficient on its face, because the Examiner has never cited to any portion of the single Ikeda reference for being analogous to the pattern data features of claim 6, or the data-synthesis circuit of claim 7, which depends from claim 6. In all three consecutive Office Actions that cite the Ikeda reference, the Examiner has not once cited to any particular portion of the reference that he deems teach these features. It is further significant that the Examiner has not once rebutted any of Applicants' several arguments in the respective Responses to these three Office Actions, which formally requested that the Examiner point to specific teachings within the Ikeda reference that he found analogous to claims 6 and 7, or withdraw the rejection. Because the Examiner has never responded to any of these formal requests either, Applicant respectfully requests that this Board should reverse the Examiner's final rejection of claims 6 and 7 for at least these reasons alone.

With respect to claim 8 of the present invention, a case of anticipation has not been established because the Examiner has not cited to any description within the single Ikeda reference to enable one skilled in the art to utilize the display-information acquisition circuit, or the display-information memories, of claim 8. The Examiner only asserts that Ikeda's address converter somehow meets all of the limitations of these two additional elements as recited in claim 8, but cites to only claim language from claim 14 of Ikeda (col. 42, lines 59-64) for support, and not to any enabling description in Ikeda's Disclosure. The brief text from claim 14 of Ikeda, however, hardly describes the particular features recited in claim 8 of the present invention.

More particularly, even if the Examiner were correct that the address converter recited in Ikeda's claim 14 could be analogous to the display information acquisition circuit of claim 8 of the present invention, nowhere does claim 14 of Ikeda also recite the particular display information memories of the present invention which store the information acquired by the acquisition circuit. The Examiner has not rebutted any of these meritorious arguments by Applicant, and this Board should therefore reverse the final rejection of claim 8 for at least these reasons.

This Board should also reverse the Examiner's final rejection of claim 9 of the present invention. Claim 9 depends from claim 8, and further recites how the display-information acquisition circuit checks the display unit of the present invention to require information with regard to a defect of the display unit. The Examiner asserts that Ikeda's two stages of latch circuits 187 and 189 meet all of the limitations of claim 9 of the present invention, but this assertion is erroneous. Ikeda only teaches, at col. 30, lines 26-32, that the two stages of latch circuits 187 and 189 are provided to enable a display operation at a fixed period, in order to keep the quality of display from deteriorating. This description alone, however, hardly meets all of the limitations specifically recited in claim 9 of the present invention.

Claim 9 does not merely recite a circuit that keeps the quality of display from deteriorating. Instead, claim 9 affirmatively recites that the acquisition circuit checks the display unit to acquire information with regard to a defect of the display unit. The cited portion of Ikeda, on the other hand, does not describe a circuit which affirmatively checks the

display unit, acquires specific information from the display unit, and that such information is in regard to a defect in the display unit. Accordingly, a *prima facie* case of anticipation has not been established against claim 9, and Applicant respectfully requests that the Board reverse the final rejection thereto.

A *prima facie* case of anticipation has similarly not been established against claim 10 of the present invention. Claim 10 also depends from claim 8, and further recites that the same acquisition circuit acquires information about the display unit with regard to coordinates of a position at which input is entered on the display unit. The Examiner, however, cites only the same general portion of Ikeda's claim 14 claiming an address converter as meeting the limitations of claim 10. The address converter recited in Ikeda's claim 14 though, does not even describe anything related to particular coordinates of a position at which input is entered on the display unit, as claimed in claim 10 of the present invention. More particularly, claim 14 provides no direction to one skilled in the art for how such a specific acquisition circuit can acquire such position coordinate information and store it in different display-information memories. These meritorious arguments have also been previously provided by Applicant, but not rebutted by the Examiner. Applicant therefore also respectfully requests that this Board reverse the Examiner's final rejection of claim 10 as well.

II. INHERENCY HAS BEEN INAPPROPRIATELY RELIED UPON AGAINST PARTICULAR FEATURES OF THE PRESENT INVENTION THAT ARE NOT DISCLOSED IN THE SINGLE PRIOR ART REFERENCE.

The Examiner appears to recognize that at least some recited limitations of the present invention are not expressly taught (or suggested) by the single Ikeda reference, but still asserts that Ikeda anticipates the present invention because such features are "inherent" to Ikeda's device. The Examiner's reliance on inherency, however, is inappropriate. The Examiner has not cited to any specific portions of the Ikeda reference to support his assertion of inherency, and Ikeda itself teaches specific alternatives which defeat the finding of inherency. Furthermore, the Examiner has provided no extrinsic evidence to otherwise support the insertion of inherency.

A. The Single Prior Art Reference Itself Does Not Support the Assertion of Inherency.

This Board, in an unpublished opinion, stated that "when an Examiner relies on inherency, it is incumbent upon the Examiner to point to the 'page and line' of the prior art which justifies an inherency theory." Ex parte Schricker, 56 USPQ 2d 1723 (BPAI 2000) (unpublished). In the present case, however, the Examiner has cited to no specific portions of the single Ikeda reference to support his assertions that display control information such as that stored in the memories of the present invention, "is inherently transmitted through the address bus." (Paper No. 22, page 6). In fact, the Ikeda reference provides no such support, and even teaches the opposite.

Those skilled in the art are well apprised that conventional devices typically transmit image display data through the data bus, image address data through the address bus, and control information for the display of such image data to its address information through the control bus. Ikeda even provides specific teachings consistent with such conventional devices. Ikeda teaches, at col. 14, lines 59-60, that display data is transferred the data bus 1605. Ikeda further teaches, at col. 14, lines 13-14, that address information is transferred through the address bus 1604. Lastly, at col. 14, lines 56-58, Ikeda teaches that the control signal bus 1611 receives an output control signal. Ikeda provides no express teachings to contradict, or somehow deviate from, this conventional configuration.

At most therefore, even if the Examiner were correct that control information *could be* transmitted through the address bus and the data bus of Ikeda, Ikeda does not clearly teach that such control information will necessarily be transmitted through the address bus. Inherency therefore, by definition, cannot be justified in the present case because the single prior art reference provides express teachings that the Examiner's proposed configuration will not be the necessary, or inherent, result.

In other words, the Examiner has not established where in the prior art his proposed inherent configuration *must* result in Ikeda. Instead, the Examiner has only provided a rationale for how such a configuration *may* result. This rationale, however, by itself, cannot establish inherency. It has been unequivocally held that "inherency may not be established by probabilities or possibilities." See In re Oelrich, 666 F.2d 578, 581, 22 UPSQ 323, 326 (CCPA 1981) ("The mere fact that a certain thing *may* result from a given set of

circumstances is not sufficient.") The Federal Circuit has even expressly ruled that "inherency is not present when prior art is *only capable of being modified*." See In re Robertson, 169 F.3d 743, 49 USPQ 2d, 1949, (Fed. Cir. 1999) (emphasis added). In the present case, the Examiner has established no more than such probabilities and possibilities.

First, the Examiner has never even established that Ikeda expressly teaches display control information, as in the present invention. As discussed above, the Examiner has only asserted that such display control information, stored in memories, "may" exist. Upon this original probability, the Examiner additionally asserts that such possible display control information *could be* possibly transmitted through the address bus and/or data bus of Ikeda as an inherent characteristic. Second though, no specific support from the reference has been provided by the Examiner to support this further assertion, other than the Examiner's own personal assurance. The Examiner's own assurances though, do not satisfy the requirements to establish an anticipation rejection, or inherency. Even assuming that the Examiner is knowledgeable in the field of art at issue, "that presumed knowledge does not grant a license to read into the prior art reference teachings that are not there." See Motorola, Inc. v. Interdigital Tech. Corp., 121 F.3d 1461, 43 USPQ 2d 1481 (Fed. Cir. 1997).

For at least these additional reasons, Applicant respectfully requests that this Board reverse the Examiner's rejection of claims 2-11 of the present invention.

B. The Examiner Has Provided No Other Extrinsic Evidence on the Record to Support the Assertion of Inherency.

Even though a reference may be silent about an asserted inherent characteristic, "such gap in the reference may be filled by extrinsic evidence," provided by the Examiner. See Continental Can Co. U.S.A. v. Monsanto Co., 948 F.2d 1264, 20 USPQ 2d 1746 (Fed. Cir. 1991). However, when such extrinsic evidence is provided, it "must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." Id. In the present case, however, no such extrinsic evidence has been provided, and even after the assertions of inherency have been several times traversed by Applicant.

The Examiner's own personal knowledge or assurances therefore cannot satisfy the requirements for objective, extrinsic evidence. See id; see also In re Lee, 277 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002) ("The patent examiner and the Board are deemed to have experience in the field of the invention; however, this experience, insofar as applied to the determination of patentability, must be applied from the viewpoint of 'the person having ordinary skill in the art to which said subject matter pertains.'"). The unsupported assertions of inherency cannot therefore be maintained.

Because inherency has been inappropriately asserted against the present invention based on the single Ikeda reference, Applicant submits that this Board should find that claims 2-11 of the present invention were improperly rejected under Section 102.

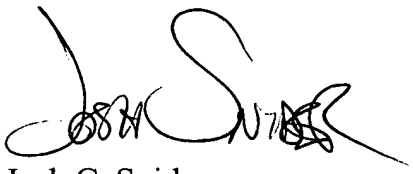
Applicant respectfully requests that the Board make such a finding.

CONCLUSION

For all of the foregoing reasons, Applicant respectfully requests that the Board reverse the Examiner's Section 102 final rejection of claims 2-11 of the present invention.

Respectfully submitted,

GREER, BURNS & CRAIN, LTD.

By 

Josh C. Snider
Registration No. 47,954

Customer No. 24978

April 11, 2005

300 South Wacker Drive
Suite 2500
Chicago, Illinois 60606
Telephone: (312) 360-0080
Facsimile: (312) 360-9315
P:\DOCS\0941\63081\739309.DOC

REJECTED CLAIMS

1. (Cancelled)

2. (Previously Presented) A display device comprising:

a display unit which displays an image;

a display-data line which supplies data of the image from an exterior to said display unit;

memories which store information for controlling displaying of the data of the image on said display unit, said information being different from said data of the image;

an operation circuit unit which controls said display unit to display the data of the image supplied through said display-data line based on the information stored in said memories;

a data bus which connects said memories to an exterior of said display device, and supplies the information to said memories from the exterior of said display device; and

an address bus which connects said memories to the exterior of said display device, and supplies address signals for selecting one of said memories,

wherein said operation circuit unit includes:

a gate driver which drives gate lines of said display unit; and

a data driver which drives data lines of said display unit, wherein at least one of said gate driver and said data driver operates based on the information sorted in said memories.

3. (Original) The display device as claimed in claim 2, wherein the at least one of said gate driver and said data driver includes a shift register which operates based on the information stored in said memories to control a scan direction of said display unit.

4. (Original) The display device as claimed in claim 2, wherein the at least one of said gate driver and said data driver includes a decoder which operates based on the information stored in said memories to control a scan direction and a scan order of said display unit.

5. (Original) The display device as claimed in claim 4, wherein the at least one of said gate driver and said data driver further includes an address counter which operates based on the information stored in said memories to supply an address to said decoder, said decoder decoding the address to control the scan direction and the scan order of said display unit.

6. (Original) The display device as claimed in claim 2, wherein said memories store pattern data, said data driver operating in accordance with the pattern data stored in said memories to control said display unit to display an image corresponding to the pattern data.

7. (Original) The display device as claimed in claim 6, wherein said operation circuit unit further includes a data-synthesis circuit which combines the pattern data stored in said memories and display data supplied from the exterior of said display device to generate synthesized pattern data, said data driver operating in accordance with the synthesized pattern data to control said display unit to display an image corresponding to the synthesized pattern data.

8. (Previously Presented) The display device as claimed in claim 2, further comprising:

a display information acquisition circuit which acquires information about said display unit; and

display-information memories which store the information about said display unit, and are connected to said data bus and said address bus so as to supply the information about said display unit to the exterior of said display device when so requested.

9. (Original) The display device as claimed in claim 8, wherein said display-information acquisition circuit checks said display unit to acquire the information about the said display unit with regard to a defect of said display unit.

10. (Original) The display device as claimed in claim 8, wherein said display-information acquisition circuit acquires the information about the said display unit with regard to coordinates of a position at which input is entered on said display unit.

11. (Original) The display device as claimed in claim 2, wherein said display unit includes:

a plurality of polysilicon thin-film transistors; and

a plurality of pixel electrodes corresponding to the respective polysilicon thin-film transistors, wherein display data is supplied to the pixel electrodes via the polysilicon thin-film transistors selected by said gate driver and said data driver.